ABSTRACT OF THE DISCLOSURE

The present invention is a dual-level flash memory cell design that stores 3 or more bits of information per transistor. The dual-level memory cell stores two lower bits in a first level and stores an upper bit in a second level. The lower bits are programmed, érased and read by alternate modes of operation wherein active regions operate as source and drain, and then drain and source. The upper bit is programmed and erased independent of the lower bits. However, reading of the upper bit depends upon read values of the lower bits. Additional levels are employed to store more than 3 bits of information.